IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A device comprising an array of pixels, each pixel including a pixel element and being associated with a switching circuit, wherein the switching circuit is for selectively routing one of at least two inputs to the pixel element, comprising at least first and second switching transistors connected between a respective one of the at least two inputs and the pixel element, wherein each switching transistor is controlled by a data signal applied to the gate of the transistor, wherein the data signal for each switching transistor is routed to the gate of the switching transistor with predetermined timing determined in dependence on the data waveform of at least one of the inputs, and wherein a capacitive connection is provided between the gate of at least one of the switching transistors and a common ~~an~~ output node of the switching transistors.

2. (Currently Amended) A device as claimed in claim 1, wherein the data signal for each switching transistor is routed to the gate of the switching transistor by a transfer switch which controls the timing of application of the data signal for each switching transistor and wherein a capacitive connection is provided between the gate of each switching transistor and the common output node ~~output of each switching transistor~~.

3. (Canceled)

4. (Currently Amended) A device as claimed in ~~any preceding~~ claim 1, wherein the gates of the first and second switching transistors are connected together and the capacitive

connection comprises a capacitor connected between the gates and the common ~~an~~ output node ~~an output of the switching circuit~~.

5. (Previously Presented) A device as claimed in claim 4, wherein the first switching transistor is an n-type transistor and the second switching transistor is a p-type transistor.

6. (Currently Amended) A device as claimed in claim 1, wherein the capacitive connection comprises a respective capacitor connected between the gate of each switching transistor and the common output node ~~an output of the switching circuit~~.

7. (Currently Amended) A device as claimed in claim 10 ~~6~~, comprising n inputs, where n is greater than 2, and comprising first to nth switching transistors connected between a respective one of the n inputs and the pixel element, and wherein the data signals for each switching transistor are selected such that an individual one of the switching transistors is turned on to route the respective input to the pixel element.

8. (Original) A device as claimed in claim 7, wherein at least one of the switching transistors is n-type and at least one of the switching transistors in p-type.

9. (Original) A device as claimed in claim 7, wherein all switching transistors are of the same polarity type.

10. (Currently Amended) ~~A device as claimed in claim 6,~~ A device comprising an array of

pixels, each pixel including a pixel element and being associated with a switching circuit, wherein the switching circuit is for selectively routing one of at least two inputs to the pixel element, comprising at least first and second switching transistors connected between a respective one of the at least two inputs and the pixel element, wherein each switching transistor is controlled by a data signal applied to the gate of the transistor, wherein the data signal for each switching transistor is routed to the gate of the switching transistor with predetermined timing determined in dependence on the data waveform of at least one of the inputs, and wherein the capacitive connection comprises a respective capacitor connected between the gate of each switching transistor and an output of the switching circuit, the device further comprising n inputs, and comprising first to nth switching transistors connected between a respective one of the n inputs and one of two intermediate outputs, and wherein the data signals for each switching transistor are selected such that half of the switching transistors are turned on to route a first selected input to one intermediate output and to route a second selected input to the other intermediate output.

11. (Previously Presented) A device as claimed in claim 10, further comprising a switching circuit for selectively routing one of the intermediate outputs to the pixel element.

12. (Currently Amended) A device as claimed in claim 1 comprising an active matrix liquid crystal display device in which the pixel elements comprise liquid crystal cells, each pixel comprising the switching circuit for routing one of two voltage ~~chive~~ drive levels to the pixel element.

13. (Currently Amended) A device as claimed in claim 12, further comprising:

a first selection switch between the common output node of the switching circuit and the liquid crystal cell of the pixel; and

a second selection switch between an analogue pixel data line and the liquid crystal cell of the pixel.

14. (Original) A device as claimed in claim 13, wherein the two voltage drive levels comprise voltages for driving the liquid crystal cell to a black and a white state.

15. (Previously Presented) A device as claimed in claim 13, wherein the control signal for selecting which one of the two voltage drive levels is to be routed to the pixel element is provided on the analogue pixel data line.

16. (Previously Presented) A device as claimed in claim 15, wherein the data signal for each switching transistor is routed to the gate of the switching transistor by a transfer switch which controls the timing of application of the data signal for each switching transistor, and wherein a capacitive connection is provided between the gate of each switching transistor and the output of each switching transistor, and wherein the transfer switch is provided between the analogue pixel data line and the gates of the first and second switching transistors.

17. (Previously Presented) A device as claimed in claim 12, further comprising:

a first selection switch between the output of the at least one of the switching transistors and the liquid crystal cell of the pixel; and

a second selection switch between an analogue pixel data line and the liquid crystal cell

of the pixel.

18. (Previously Presented) A device as claimed in claim 17, wherein the second selection switch comprises the other of the first and second switching transistors.

19. (Previously Presented) A device as claimed in claim 18, wherein in a first mode, the second selection switch provides one of two digital pixel signals from the analogue pixel data line to the liquid crystal cell, and in a second mode the second selection switch provides an analogue pixel signal from the analogue pixel data line to the liquid crystal cell.

20. (Currently Amended) A method of routing one of at least two inputs to a pixel element within a pixel of a device comprising an array of pixels, the method comprising:

applying data signals to the gates of at least first and second switching transistors connected between a respective one of the at least two inputs and the pixel element to turn on a selected one of the first and second switching transistors and turn off the other of the first and second switching transistor, thereby routing the respective input to the pixel element,

wherein the timing of application of the data signals is selected in dependence on the signals on at least one of the two inputs,

wherein a capacitive connection is provided between the gate of at least one switching transistor and ~~an output of the~~ a common output node of the switching transistors, and

wherein the timing is controlled such that the capacitive connection reduces the required voltage swing in the data signal between that required to turn on and turn off a switching

transistor.

21. (Original) A method of driving a liquid crystal display, comprising:

in a first mode, switching analogue pixel drive signals to each pixel of the display; and

in a second mode, routing one of two pixel drive signals on respective inputs to each pixel of the display, the routing for each pixel in the second mode using the method of claim 20.